APPENDIX C
complete set of "clean" claims
pursuant to 37 C.F.R. §1.121(c)(3)

1. A trench-type power MOSFET having a vertical invertible channel composed of N type conductivity material and disposed between a source region and a drain region; a gate oxide and gate contact thereon extending along the length of said invertible channel and operable to invert the conductivity type of said invertible channel; said gate contact containing a P type conductivity material; said vertical invertible channel material having a constant concentration along its full length.

2. The power MOSFET of claim 1 wherein said one of the conductivity types is the N-type.

3. The power MOSFET of claim 1 wherein said invertible channel material is epitaxially deposited silicon.

4. A power MOSFET comprising, in combination; a P type substrate; an epitaxially deposited N type layer deposited atop said substrate and having a substantially constant concentration; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive P type polysilicon deposited into said trenches to define a polysilicon gate; a P type source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; a drain contact connected to said substrate; whereby said MOSFET has a reduced on resistance.

5. The MOSFET of claim 4 wherein said source contact is connected to said source region only, whereby said MOSFET is bidirectional.

6. The MOSFET of claim 4 wherein said source contact is connected to said epitaxially deposited layer.

7. The MOSFET of claim 4 wherein said one conductivity type is the P-type.

8. The MOSFET of claim 7 wherein said epitaxial region has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

9. A power MOSFET having reduced on resistance comprising, in combination; a P type conductivity substrate; an epitaxially deposited N type conductivity layer deposited atop said P type substrate to form an epitaxial layer having a substantially constant concentration throughout its volume; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; a P type concentration source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; and a drain contact connected to said substrate.

10. The MOSFET of claim 9 wherein said source contact is connected to said epitaxially deposited layer.

11. The MOSFET of claim 10 wherein said epitaxial layer has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

12. The MOSFET of claim 9 wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

13. The MOSFET of claim 10 wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

20. A trench-type power MOSFET according to claim 1, further having highly doped contact regions at a top portion of said vertical invertible channel.

21. A power MOSFET according to claim 4, further comprising highly doped contact regions in said epitaxial layer.

22. A power MOSFET having reduced on resistance according to claim 9, further comprising highly doped contact regions in said epitaxial layer.